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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/681,254	10/09/2003	Ki-Myung Yoon	2557-000171/US	7505

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EXAMINER	
TRAN, DUE NGOC	
ART UNIT	**PAPER NUMBER**
2841	

DATE MAILED: 09/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)	
Office Action Summary	10/681,254	YOON, KI-MYUNG	
	Examiner	**Art Unit**	
	Due N. Tran	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date *2/17/2005*.

4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Londa (U.S 6,101,100) in view of Mostafazadeh et al (U.S 5,783,870).

2. With respect to claim 1, Londa discloses a multi-chip semiconductor package comprising: a plurality of stacked semiconductor package structures (Fig. 2), each semiconductor package structure including; a substrate having an upper surface (Fig. 2 element 12) and a lower surface (Fig.2 element 22), a semiconductor chip mounted on the substrate (Fig.2 element 36), the semiconductor chip including an active surface (Fig. 2 element 16) and a backside surface (Fig. 2 element 14); a plurality of conductive studs extending through the enclosure body outside a periphery of the semiconductor chip (Fig.2 elements 42,44,46), the conductive studs having an upper surface (Fig. 2 element 12) and a lower surface (Fig.2 element 22); and at least one conductive member formed in contact with the lower surface of at least one of the conductive studs (Fig. 2 element 42 and page 10, col. 4, lines 15-19), however, Londa does not disclose

expressly wherein the multi-chip has an enclosure body covering substantially the entire upper surface of the substrate.

The Mostafazadeh reference, however, discloses a multi-chip having an enclosure body covering substantially the entire upper surface of the substrate (Fig. 4a element 32).

Londa and Mostafazadeh are analogous art because they are from the same field of endeavor (Multi-chip package).

At the time the invention, it would have been obvious to a person of ordinary skill in the art to modify the enclosure of Londa by having the enclosure covering the entire upper surface of the substrate.

The suggestion or motivation for doing so would have been obvious in view of the teaching of Mostafazadeh in preventing of trapping heat and raising the stress within the package.

Therefore, it would have been obvious to combine Mostafazadeh with Londa for the benefit to prevent the thermally induced failures, which is cause by trapping heat.

3. With respect to claim 2, Londa discloses a multi-chip semiconductor package wherein the stacked semiconductor package structures include an upper package structure and a lower package structure, the upper package structure and the lower package structure having substantially the same configuration (Fig. 2); wherein the at least one conductive member of the upper package structure is in electrical contact with at least one conductive stud of the lower package structure (Fig. 2 element 42 and page 10, col. 4, lines 15-19).

4. With respect to claim 3, Londa discloses a multi-chip semiconductor package wherein the stacked semiconductor package structures include an upper package structure and a lower package structure, the upper package structure and the lower package structure having substantially the same configuration (Fig. 2); wherein the at least one conductive member of the upper package structure is in direct electrical contact with the at least one conductive member of the lower package structure (Fig. 2, the upper stud is electrical contact with lower stud through the solder 90).

5. With respect to claim 4, Londa discloses a multi-chip semiconductor package wherein the substrate includes a conductive layer (Fig. 2 element 30 and page 10, col. 3, lines 51-53), the conductive layer having an upper surface (Fig. 2 element 32) and a lower surface (Fig. 2, element 34), and an insulating layer, the insulating layer being formed on the lower surface on the conductive layer (Fig. 2 element 22 and page 10, col. 3, lines 48-50).

6. With respect to claim 5, Londa discloses a multi-chip semiconductor package wherein the active surface of the semiconductor chip includes conductive pads, the conductive pads being electrically connected to the conductive layer (Fig. 2 element 36 and page 10, col. 3, lines 61-63).

7. With respect to claim 6, Londa discloses a multi-chip semiconductor package wherein backside surface of the semiconductor chip is recessed below a plane defined by the upper surface of the conductive layer (Fig. 2).

8. With respect to claim 7, Londa discloses a multi-chip semiconductor package wherein the active surface of the semiconductor chip is substantially coplanar with or recessed below the plane defined by the upper surface of the conductive layer (Fig. 2).

9. With respect to claim 8, Londa discloses a multi-chip semiconductor package wherein conductive balls are formed on a plurality of bond pads on the active surface of each semiconductor chip, the conductive balls providing direct electrical contact to the conductive layer (Fig. 2 element 36 and page 10, col. 3, lines 36-39).

10. With respect to claim 9, Londa discloses a multi-chip semiconductor package wherein the at least one conductive member includes a plurality of solder balls (Fig. 2 element 66, 68, 70).

11. With respect to claim 10, Londa discloses a multi-chip semiconductor package wherein the at least one conductive member includes a conductive pattern (Fig. 2 element 66, 68, 70).

12. With respect to claim 11, Londa discloses a multi-chip semiconductor package wherein the substrate includes conductive layer Fig. 2 element 30 and page 10, col. 3, lines 51-53), the conductive layer having an upper surface (Fig. 2 element 32) and a lower surface (Fig. 2 element 34), and an insulating layer formed on the upper surface of the conductive layer (Fig. 2 element 12); and further wherein a second plurality of conductive studs extend through the insulating layer and are electrically connected to corresponding ones of the plurality of conductive studs extending through the enclosure body (Fig. 2 element 42, 44, 46).

13. With respect to claim 12, Londa discloses a multi-chip semiconductor package comprising: an upper semiconductor package structure and a lower semiconductor package structure (Fig. 2), each semiconductor package structure including; a substrate having an upper surface (Fig. 2 element 12) and a lower surface (Fig. 2 element 22) and including a conductive layer (Fig. 2 element 30) and an insulating layer (Fig. 2 element 30); a semiconductor chip mounted on the substrate (Fig. 2 element 36), the semiconductor chip including an active surface (Fig. 2 element 16)and a backside surface (Fig. 2 element 14); a plurality of conductive studs extending through the enclosure body outside a periphery of the semiconductor chip (Fig. 2 elements 42, 44, 46), the conductive studs having an upper surface (Fig. 2 element 12) and a lower surface (Fig. 2 element 22); wherein at least one conductive member is formed in contact with the lower surface of at least one of the conductive studs of the upper semiconductor package structure (Fig. 2 element 42 and page 10, col. 4, lines 15-19); and the upper semiconductor package structure and the lower semiconductor package structure are positioned so that the at least one conductive member is in electrical contact with the upper surface of at least one conductive stud of the lower semiconductor package structure (Fig. 2, the upper stud is electrical contact with lower stud through the solder 90), however, Londa does not disclose expressly wherein the multi-chip has an enclosure body covering substantially the entire upper surface of the substrate.

The Mostafazadeh reference, however, discloses a multi-chip having an enclosure body covering substantially the entire upper surface of the substrate (Fig. 4a element 32).

Londa and Mostafazadeh are analogous art because they are from the same field of endeavor (Multi-chip package).

At the time the invention, it would have been obvious to a person of ordinary skill in the art to modify the enclosure of Londa by having the enclosure covering the entire upper surface of the substrate.

The suggestion or motivation for doing so would have been obvious in view of the teaching of Mostafazadeh in preventing of trapping heat and raising the stress within the package.

Therefore, it would have been obvious to combine Mostafazadeh with Londa for the benefit to prevent the thermally induced failures, which is cause by trapping heat.

14. With respect to claim 13, Londa discloses a multi-chip semiconductor package wherein the at least one conductive member includes a plurality of solder balls formed on the lower surfaces of a plurality of the conductive studs of the upper semiconductor package structure (Fig. 2 elements 90, 92, 94); and the plurality of solder balls are in electrical contact with the upper surfaces of corresponding conductive studs of the lower semiconductor package structure (Fig. 2 and page 10 col. 4, lines 15-19).

15. With respect to claim 14, Londa discloses a multi-chip semiconductor package wherein the semiconductor chip is mounted in a recessed orientation in which the

backside surface lies below a plane defined by the upper surface of the substrate (Fig. 2).

16. With respect to claim 15, Londa discloses a multi-chip semiconductor package wherein the insulating layer includes a resin material (page 10, col. 3, lines 48-50) and the conductive layer includes a metallic material (page 10, col. 3, lines 55-59).

17. Regarding to method claims 16- 21, one skill in the art would necessarily perform the recited method steps in manufacturing a multi-chip semiconductor package rejected above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Due N. Tran whose telephone number is (571) 272-5984. The examiner can normally be reached on Monday-Thursday, 9:00am-6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

KAMAND CUNEO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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